What is claimed is:

[Claim 1] 1. A method for connecting low pin count (LPC, hereinafter) bus to serial flash memory, comprising:

(a) fetching a LPC bus instruction;
(b) converting the LPC bus instruction to a serial instruction according to the required format of a serial flash memory;
(c) provided the serial instruction is a write instruction, recording the serial instruction, accumulating write instructions until N instructions are received, combining the accumulated instructions and outputting to a serial flash memory at one time, where N is a preset positive integer;
(d) provided the serial instruction is a read instruction, reading M bytes of data from the serial flash memory and outputting the data sequentially, where M is a preset positive integer;
(e) converting an output data to the required format according to the LPC bus, where the output data is for responding to the LPC bus instruction; and
(f) outputting the output data of converted format to the LPC bus.

[Claim 2] 2.The method for connecting LPC bus and serial flash memory as recited in claim 1, further comprising:

calculating a cycle count of a clock signal provided by the LPC bus instruction, for identifying a command field, an address field, and a data field of the serial instruction.

[Claim 3] 3.The method for connecting LPC bus and serial flash memory as recited in claim 1, wherein the procedure (c) comprises:

recording the data field of the serial instruction and the data field of a plurality of former write instructions; and
provided N data fields are accumulated and recorded, outputting the command field and the address field of the serial instruction to the serial flash memory, and outputting the recorded data field to the serial flash memory according to the sequence of recording.

[Claim 4] 4.The method for connecting LPC bus and serial flash memory as recited in claim 1, wherein M is a preferred setting equivalent to the efficient size of a central processing unit (CPU, hereinafter) process divided by 8.

[Claim 5] 5.The method for connecting LPC bus and serial flash memory as recited in claim 1, wherein N is a preferred setting equivalent to the efficient size of a CPU process divided by 8.

[Claim 6] 6.A method for connecting low pin count (LPC) bus and serial flash memory, comprising:

(a) fetching an LPC bus instruction;
(b) converting the LPC bus instruction to a serial instruction according to the required format of a serial flash memory;
(c) outputting the serial instruction to a serial flash memory; and
(d) receiving an output data outputted from the serial flash memory, converting the format of the output data, and outputting the output data of converted format to the LPC bus.

[Claim 7] 7.The method for connecting LPC bus and serial flash memory as recited in claim 6, further comprising:

calculating a cycle count of a clock signal provided by the LPC bus instruction, for identifying a command field, an address field, and a data field of the serial instruction.

[Claim 8] 8.The method for connecting LPC bus and serial flash memory as recited in claim 6, wherein the procedure (d) comprises:

provided the serial instruction is a read instruction, reading M bytes of data from the serial flash memory at one time, and outputting the data sequentially, wherein M is a preset positive integer;
converting the data to the required format according to the LPC bus; and
outputting the data of converted format to the LPC bus.

[Claim 9] 9.The method for connecting LPC bus and serial flash memory as recited in claim 8, wherein M is a preferred setting equivalent to the efficient size of a CPU process divided by 8.

[Claim 10] 10.The method for connecting LPC bus and serial flash memory as recited in claim 6, wherein provided the serial instruction is a write instruction, the procedure (c) comprises:

recording the data field of the serial instruction and the data field of a plurality of former write instructions; and

provided N data fields are accumulated and recorded, outputting the command field and the address field of the serial instruction to the serial flash memory, and outputting the recorded data to the serial flash memory according to the sequence of recording, where N is a preset positive integer.

[Claim 11] 11.The method for connecting LPC bus and serial flash memory as recited in claim 10, wherein N is a preferred setting equivalent to the efficient size of a CPU process divided by 8.

[Claim 12] 12.An apparatus for connecting low pin count (LPC) bus and serial flash memory, comprising:

a latch, for registering and outputting a LPC bus instruction transmitted from a LPC bus;

an instruction converter, for receiving the LPC bus instruction outputted from the latch, converting the LPC bus instruction to a serial instruction according to the required format of serial flash memory, and outputting the serial instruction;

a parallel to serial converter, for receiving and recording the serial instruction outputted from the instruction converter, provided the serial instruction is a read instruction, accumulating and recording M read instructions, combining the read instructions, and converting the combined instruction from parallel signals to serial signals for output, provided the serial instruction is a write instruction, accumulating and recording N write instructions, combining the write instructions, and converting the combined instruction from parallel signals to serial signals for output, where M and N are both preset positive integer;

a serial output device, for coupled in between the parallel to serial converter and a serial flash memory, outputting the serial signals outputted from the parallel to serial converter to the serial flash memory; and

a serial to parallel converter, for receiving an output data which is needed for responding to the LPC bus instruction from the serial flash memory, converting the output data to the required format according to the LPC bus, and outputting the output data of converted format to the LPC bus.

[Claim 13] 13.The apparatus for connecting LPC bus and serial flash memory as recited in claim 12, wherein the instruction converter further comprises:

a command decoder, for coupled in between the latch and the parallel to serial converter, converting the command field of the LPC bus instruction to a command field of the serial instruction;
an address compare multiplexer, for coupled in between the latch and the parallel to serial converter, converting the address field of the LPC bus instruction to an address field of the serial instruction; and
a data compare multiplexer, for coupled in between the latch and the parallel to serial converter, converting the data field of the LPC bus instruction to a data field of the serial instruction.

[Claim 14] 14.The apparatus for connecting LPC bus and serial flash memory as recited in claim 12, further comprising:

a counter, for receiving a clock signal provided by the LPC bus, calculating a cycle count of the clock signal, and outputting the cycle count to the parallel to serial converter and to the serial to parallel converter for identifying the command field, the address field, and the data field in the serial instruction.

[Claim 15] 15.The apparatus for connecting LPC bus and serial flash memory as recited in claim 12, wherein the serial to parallel converter further comprises:

a read register, when the serial instruction is a read instruction, for receiving M bytes of data from the serial flash memory at one time, converting the format of the data sequentially, and outputting to the LPC bus.

[Claim 16] 16.The apparatus for connecting LPC bus and serial flash memory as recited in claim 12, wherein the parallel to serial converter further comprises:

a batch read device, for receiving the command field and the address field of the serial instruction, and issuing instructions for reading M bytes of data from the serial flash memory at one time;
a write register, provided the serial instruction is a write instruction, for receiving the data field of the serial instruction, storing the data field of the serial instruction and the data field of former N-1 write instructions, and outputting the data fields according to the sequence of stores; and
a batch write device, for receiving the output data field from the write register, and receiving the command field and the address field of the serial instruction, provided the serial instruction is a write instruction, outputting the command field and the address field of the serial instruction as well as the data fields to the serial flash memory.

[Claim 17] 17.The apparatus for connecting LPC bus and serial flash memory as recited in claim 12, wherein M is a preferred setting equivalent to the efficient size of a CPU process divided by 8.

[Claim 18] 18.The apparatus for connecting LPC bus and serial flash memory as recited in claim 12, wherein N is a preferred setting equivalent to the efficient data of a CPU process divided by 8.